REMARKS

Claims 1-28, 44-63, and 79-105 are now pending in the application. Claims 29-43, 64-78, and 106-120 are cancelled without disclaimer or prejudice to the subject matter contained therein. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 112

Claims 1-11, 13-15, 20, 79, 80-89, 91-93 and 97 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point and distinctly claim the subject matter which Applicants regard as the invention. This rejection is respectfully traversed.

With respect to claim 1, the Examiner alleges that the recitation "when said line cache receives said first address" in lines 18-20 is unclear. Applicants amended claim 1 to recite "wherein when said line cache receives said second address, said line cache compares said second address to stored addresses in said line cache, returns data associated with said second address if a match occurs, and retrieves data from one of the first and second memory devices if a miss occurs." Applicants respectfully submit that claim 1 is now definite.

With respect to claim 6, Applicants amended line 5 to recite "a third address." Applicants respectfully submit that claim 6 is now definite.

With respect to claim 79, the Examiner alleges that lines 16-19 recite "said line cache means receives said first address." Applicants respectfully note that the cited portion of claim 79 recites "wherein when said line cache means receives said

translated address, said line cache means compares said translated address to stored addresses in said line cache means, returns data associated with said translated address if a match occurs, and retrieves data from one of the first and second memory means if a miss occurs." Applicants respectfully submit that it is clear that the line cache means receives the translated address, and that claim 79 is definite.

REJECTION UNDER 35 U.S.C. § 103

Claims 1-5, 11, 13-15, 20, 44-48, 50, 52-54, 79-83, 89, 91-92 and 97 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1) and Jim Handy (The Cache Memory Book, second edition, published 1998) and Taylor et al. (U.S. Pat. No. 5,699,551). Claims 16-18, 32-38, 55-57, 67-73, 93-95 and 109-115 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1), Jim Handy (The Cache Memory Book, second edition, published 1998) and Taylor et al. (U.S. Pat. No. 5,699,551) in further view of Bryant et al. (U.S. Pat. No. 4,008,460). Claims 19, 58 and 96 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1), Jim Handy (The Cache Memory Book, second edition, published 1998),Taylor et al. (U.S. Pat. No. 5,699,551) and Barroso et al. (U.S. Pat. No. 6,725,334 B2) in further view of Veidenbaum et al. (Adapting Cache Line Size to Application Behavior, pub. 1999). Claims 12, 29, 39, 51, 64, 74, 90, 106 and 116 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1), Jim Handy (The Cache Memory Book, second edition, published 1998),Taylor et al. (U.S. Pat. No.

5,699,551) and Barroso et al. (U.S. Pat. No. 6,725,334 B2) in further view of Ebner et al. (U.S. Pat. No. 6,928,525). These rejections are respectfully traversed.

With respect to claim 1, Zaidi, either singly or in combination with any of the other cited prior art references, fails to show, teach, or suggest that said switch includes a plurality of selectors that each receive the second address and each select between first and second sets of signals relating to the first and second memory devices, respectively, based on the second address.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, alleged combination fails to disclose the limitation that the switch includes a plurality of selectors that each select between first and second sets of signals relating to the first and second memory devices based on the second address.

As shown in exemplary embodiments in FIGS. 6 and 7 of the present application, a line cache 230 communicates with first and second memory (e.g. a buffer memory and a flash memory) interfaces via a switch 268. The switch 268 receives a second (i.e. translated) address and selectively connects the line cache 230 to the memory interfaces. For example, as shown in FIG. 6, a first multiplexer/selector 244 receives a memory select signal lc_addr[24] and selects between a buffer clock signal bf_clk and a flash clock signal f_clk accordingly. A second multiplexer/selector 246 receives the

memory select signal lc_addr[24] and selectively outputs a signal to a buffer interface or a flash interface. A third multiplexer/selector 248 receives the memory select signal lc_addr[24] and selects between buffer and flash acknowledgment signals.

In other words, the switch includes a plurality of selectors that each select between first and second sets of signals relating to the first and second memory devices based on the memory select signal (e.g. based on the second address). As best understood by Applicants, Zaidi fails to disclose this limitation.

For example, the Examiner appears to rely on FIG. 1 of Zaidi to disclose the switch (MAC 140). Applicants respectfully note that neither FIG. 1 nor any other figure of Zaidi appears to disclose the structure of a plurality of selectors as Applicants' claim 1 recites. Zaidi appears to disclose that the MAC 140 receives addressing information over bus 130, for example, and communicates with the memory devices 106 and 108 over bus 104. The MAC 140 is not shown to include a plurality of selectors that each receive a memory select signal and select between sets of signals relating to the memory devices 106 and 108 based on the memory select signal.

Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. The remaining independent claims, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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